VARIABLE GAIN AMPLIFIER

1. FIELD OF THE INVENTION

[0001] The present invention relates to an operational amplifier, and more particularly, to a variable gain amplifier.

2. BACKGROUND OF THE INVENTION

[0002] Please refer to Fig. 1, which is a schematic diagram depicting the framework of a conventional variable gain amplifier 100. The variable gain amplifier 100 has an operational amplifier 110, a resistor set 120 having a plurality of serial-connected resistors Rf1, Rf2, ···, Rfn, and a switch set 130 having a plurality of switches SW1, SW2, ···, SWn corresponding to the resistors respectively. The switches are generally implemented with MOS transistors. Under such configuration of Fig. 1, a gain G of the variable gain amplifier 100 is given by: $G = 1 + {Rf}/{Rg}$, wherein Rf is a resistance seen between the output Vo and the inverting input (-) of the operational amplifier 110, while Rg is a resistance seen between the inverting input (-) of the operational amplifier 110 and a ground node Vag. Both the resistance Rf and Rg depend on the on/off state of the corresponding switches in the switch set 130. The conventional variable gain amplifier 100 can ensure a monotonic variation in gain, and can avoid nonlinear distortion and gain error caused by the MOS switches since there is no current flowing through the MOS switches.

[0003] However, since the signal at the non-inverting input (+) of the operational amplifier 110 varies with the input signal Vi and the input dynamic range of the operational amplifier 110 is comparatively small, the conventional variable gain amplifier 100 tends to suffer from more significant distortion. In addition, the conventional variable gain amplifier 100 cannot perform signal attenuation and possesses inferior gain accuracy.

[0004] Please refer to FIG. 2, which is a schematic diagram depicting the

framework of another conventional variable gain amplifier 200. The variable gain amplifier 200 has an operational amplifier (OPA) 210, an input resistor Ri, a feedback resistor set 220 having a plurality of serial-connected resistors Rk1, Rk2, ···, Rkn, and a switch set 230 having a plurality of switches Sk1, Sk2, ···, Skn corresponding respectively to the resistors. The switches are generally implemented with MOS transistors. Under such configuration of Fig. 2, a gain G of the variable gain amplifier 100 is given by: $G = Rk/Ri$, wherein Rk is an equivalent resistance shown by the resistor set 220. As seen in Fig. 2, the non-inverting input (+) of the OPA 210 is fixed to a ground node Vag. Therefore, the OPA 210 tends to have smaller distortion.

[0005] However, since current will flow through the MOS switches in this framework, the nonlinearity of the MOS switch may incur signal distortion. Also, gain error may be induced by the impedance of the MOS switch. In addition, in Fig. 2 if the tolerable noise level is low, the input resistor Ri with a small impedance and the feedback resistors with small impedances are needed. However, when the impedances of the input resistor and the feedback resistors are of small values, the MOS switches with large equivalent resistances is required so as to reduce distortion and gain error. Unfortunately, when large-resistance MOS switches are adopted, the parasitic capacitors thereof tend to cause loop instability and substrate coupling issues.

SUMMARY OF THE INVENTION

[0006] It is one of the many objects of the present invention to provide a variable gain amplifier capable of amplifying and attenuating the received signals with the characteristics of low distortion and low noise.

[0007] According to embodiments of the present invention, a variable gain amplifier is disclosed. The variable gain amplifier comprises an input resistor coupled to an input signal; an operational amplifier comprising a pre-drive stage coupled to the input resistor and a plurality of output stages,

each of which coupled to the pre-drive stage; and a plurality of feedback resistors, each feedback resistor being coupled to the pre-drive stage by one end thereof and coupled to one of the plurality of output stages by another end thereof. A feedback loop is formed by one of the output stages chosen by a first control signal and the feedback resistor corresponding to the chosen output stage.

[0008] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is a framework of a conventional variable gain amplifier.

[0010] FIG. 2 is a framework of another conventional variable gain amplifier.

[0011] FIG. 3 is a schematic diagram of a variable gain amplifier according to an embodiment of the present invention.

[0012] FIG. 4 is a schematic diagram of a variable gain amplifier according to another embodiment of the present invention.

[0013] FIG. 4A is a schematic diagram of a variable gain amplifier according to yet another embodiment of the present invention.

[0014] FIG. 5 is an embodiment of the switch of FIG. 4.

[0015] FIG. 6 is an embodiment of the operational amplifier of the operational amplification unit with reference to FIG. 4.

[0016] FIG.7 is an embodiment of the output stage of the operational amplifier with reference to FIG. 4.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0017] According to embodiments of the present invention, variable gain amplifiers comprising operational amplifiers and resistors are disclosed. The variable gain amplifier may comprise an input resistor, a pre-drive stage of an operational amplifier, a plurality of output stages of the operational amplifier and a plurality of feedback resistors each coupled respectively to a corresponding output stage. In one embodiment of the present invention, the pre-drive stage, the output stages and the feedback resistors may be lumped on a single integrated circuit (IC), and the input resistor may either be integrated on the same IC or be disposed externally. One end of each input resistor is connected to the input signal, and the other end thereof is connected to an input pad of the IC. In another embodiment, the input resistor may be connected to the IC by way of an electrostatic discharge (ESD) protection device so as to prevent the damage to the variable gain amplifier from happening while the magnitude of the received signal is too large.

[0018] In one embodiment of the present invention as seen in Fig.3, a variable gain amplifier 300 comprises an operational amplifier 310, an input resistor Ri, and a plurality of feedback resistors Rf1, Rf2, ···, Rfn. The operational amplifier 310 further comprises a pre-drive stage 312, and a plurality of output stages 3141, 3142, ···, 314n. The non-inverting output of the pre-drive stage 312 is connected to the non-inverting inputs of the plurality of output stages 3141, 3142, ···,314n, and the inverting output of the pre-drive stage 312 is connected to the inverting inputs of the plurality of output stages 3141, 3142, ···, 314n. Each output stage 314i is coupled to a corresponding feedback resistor Rfi and also is coupled to a corresponding control signal Cti, where i=1,···, n. The output of each output stage 314i is coupled to the inverting input of the pre-drive stage 312 via a corresponding feedback resistor Rfi. One end of the input resistor Ri is connected to the input signal Vi, and the other end of the input resistor Ri is connected to an input pad and is further connected to the inverting input of the pre-drive stage 312 via an ESD 330.

[0019] Controlled by the control signals Ct1, Ct2, ···, Ctn, a gain G of the

operational amplifier 300 is determined by the output stage 314i chosen and driven by the foregoing control signals accompanying the feedback resistor Rfi coupled thereto, and is given as: $G = {Rfi}/{Ri}$. It is noted that the resistances of the feedback resistors are properly predetermined according to design requirement so as to provide different gain values with different output stages being chosen. Thus, the gain G of the variable gain amplifier 300 can be adjusted as desired and the received signal can be amplified/attenuated by employing the control of the output stages. In this regard, the phenomena of loop instability and substrate coupling, as well as non-linear distortion can be alleviated. Hence, the variable gain amplifier 300 can be utilized in applications demanding very low noise level, such as the asymmetric digital subscriber line (ADSL) communication system.

[0020] Please refer to Fig. 4, which is a schematic diagram of a variable gain amplifier 400 according to another embodiment of the present invention. The variable gain amplifier 400 comprises a first stage operational amplification unit 410 and a second stage operational amplification unit 420, in which the first stage operational amplification unit 410 is used for coarse gain adjustment and the second stage operational amplification unit 420 is used for fine gain adjustment. By adopting the two-stage gain adjustment approach, since the input referred noise of the second stage operational amplification unit 420 can be far higher than that of the first stage operational amplification unit 410, both input resistors with larger resistances and feedback resistors with larger resistances can be adopted, and MOS switches with smaller resistances can also be used, without causing obvious non-linear distortion and gain error.

[0021] The first stage operational amplification unit 410 as seen in Fig. 4 comprises an operational amplifier 412, a input resistor Ri and a plurality of feedback resistors 4131, 4132, ···, 413n. The operational amplifier 410 comprises a pre-drive stage 411, and a plurality of output stages. 4131, 4132, ···,413n. Each output stage 413i is controlled by a corresponding control signal Cti, where i=1,···,n. As those skilled in the art can appreciate, the first stage operational amplification unit 410 in Fig. 4 is similar to the variable gain amplifier 300 in Fig. 3, and detailed description is thus omitted

herein for simplicity.

[0022] The second stage operational amplification unit 420 as seen in Fig. 4 comprises an operational amplifier 422, a plurality of input resistors Rs1, Rs2, ···, Rsn, a plurality of switches Sw1, Sw2, ···, Swn corresponding respectively to each input resistor, a plurality of feedback resistors Rk1, Rk2, ···, Rkn, and a plurality of switches Sk1, Sk2, ···, Skn corresponding respectively to each feedback resistor. Each input resistor Rsi is coupled to the inverting input of the operational amplifier 422 by way of the corresponding switch Swi, wherein every switch Swi is controlled by a control signal Cti of the first stage operation amplification unit 410, wherein i=1, 2, ···, n. The non-inverting input of the operation amplifier 422 is connected to a virtual ground Vag. The output of the operational amplifier 422 is coupled to the inverting input thereof by way of the feedback resistors Rk1, Rk2, ···, Rkn and the corresponding switches Sk1, Sk2, ···, Skn.

[0023] In this embodiment, the first stage operational amplification unit 410 is used for coarse gain adjustment and the second stage operational amplification unit 420 is used for fine gain adjustment, where the overall operation process is illustrated using the following example. Initially, one output stage out of the output stages 4131, 4132,···, 413n, that is chosen by the plurality of control signals Ct1, Ct2, ···, Ctn, is couple to the pre-drive stage 414, for enabling a gain Gc of the first stage amplification unit 410, which is also the coarse gain of the overall variable gain amplifier, to be $Gc = {Rfi}/{Ri}$, wherein Rfi is the resistance of the feedback resistor corresponding to the chosen output stage. It is noted that the framework of the second stage amplification unit 420 is similar to that of the aforementioned variable gain amplifier with reference to Fig. 2 and the corresponding description. Thus, the fine gain Gf of the second operational amplification unit 420 is determined by the MOS switch Swi corresponding to the chosen output stage and a selected switch Ski. Finally, the total gain of the variable gain amplifier 400 is $G = Gc \times Gf$.

[0024] The adjustment ranges of both the coarse gain and the fine gain can be varied as desired. For instance, the adjustment range of the coarse gain

Gc depends, among other factors, on the number of the output stages 413i, i=1,···,n and the corresponding feedback resistors Rfi, i=1,···,n. Similarly, the adjustment range of the fine gain Gf depends, among other factors, on the number the feedback resistors Rki, i=1,···,n and the corresponding Ski, i=1,···,n. Thereby the present invention has good design flexibility for fulfilling all kinds of requirement.

[0025] For example, when designing a low-noise variable gain amplifier with -18dB ~ 23dB gain range having 1dB step, the variable gain range of the first stage amplification unit 410 may be set to be -18dB~18dB with 6dB step, and the variable gain range of the second stage amplification unit 420 may be set to be 0dB~5dB having 1dB step. Assuming that the first stage input impedance Ri is 1kΩ, then seven feedback resistors Rf1, Rf2,···, Rf7 are required in the first stage operational amplification unit 410 since the variable gain range is -18dB ~18dB with 6dB step, wherein resistances of the seven feedback resistors are 125Ω, 250Ω, 500Ω,1kΩ, 2kΩ, 4kΩ, 8kΩ, respectively. All the second stage input impedance Rs1, Rs2,···, Rs7 are then set to be 20kΩ. Six feedback resistors Rk1, Rk2,···, Rk6 are required in the second stage operational amplification unit 420 since the variable gain range is 0dB ~5dB with 1dB step, wherein resistances of the six feedback resistors are 20kΩ, 2kΩ, 3kΩ,3kΩ, 4kΩ, 4kΩ.

[0026] Please refer to Fig. 4A, which is a schematic diagram of a variable gain amplifier according to yet another embodiment of the present invention. The variable gain amplifier 400 has a first stage operational amplification unit 410 and a second stage operational amplification unit 420, which both are basically similar to those of Fig. 4. The difference between the embodiment of Fig. 4 and the embodiment of Fig. 4A is that the plurality of input resistors Rsi, i=1,···,n, are replaced by a single input resistor Rs. As a result, the adjustment range of the fine gain of the second stage amplification unit 420 depends, among other factors, on the number the feedback resistors Rki, i=1,···,n, and the corresponding switches Ski, i=1,···,n.

[0027] FIG. 5 is an embodiment of the switches of FIG. 4. As seen in Fig. 5, the switch 510 comprises a transmission gate configuration composed of

two MOS transistors. A PMOS transistor and an NMOS transistor are controlled to turn on/off by a signal SwiB and a complementary signal Swi thereof, respectively. The switch 510 composed of the two MOS transistors is illustrated as a circuit structure 520. When referencing to the aforementioned embodiments, the signal Swi of the switch 510 is the respective control signal Cti of the operational amplification unit 410.

[0028] Please refer to Fig. 6, which is an embodiment of an operational amplifier 610 used in the operational amplification unit 410. The operational amplifier 610 comprises a pre-drive stage 612 and a chosen output stage 614.

[0029] FIG.7 is an embodiment of the output stage 614 of the operational amplifier 610 illustrated by an output stage 710 and a circuit symbol thereof 720. The output stage 710 comprises two output MOS transistors Mon, Mop, and four MOS switches Msw1, Msw2, Msw3 and Msw4, wherein the transistor Mon is a N-type transistor and the transistor Mop is a P-type transistor. The MOS switches Msw1 and Msw4 are controlled by the control signal Cti, while the MOS switches Msw2 and Msw3 are controlled by the complementary signal CtiB of the control signal Cti.

[0030] When the output stage 710 is chosen, that is, in this embodiment, the control signal Cti being set to high, the MOS switches Msw1 and Msw2 are on and the MOS switches Msw3 and Msw4 are off, and the output stage 710 is therefore activated.

[0031] While the preferred embodiment of the invention has been set forth for the purpose of disclosure, modifications of the disclosed embodiment of the invention as well as other embodiments thereof may occur to those skilled in the art. Accordingly, the appended claims are intended to cover all embodiments which do not depart from the spirit and scope of the invention.